AMENDMENT TO THE CLAIMS

1. (Currently amended) A processor for handling data of multiple sizes, the processor comprising:

manipulation means for performing a manipulation on an operand, the manipulation and the operand both being specified by an instruction, the manipulation means having a bit width corresponding to a maximum one of the multiple sizes; and

manipulation control means for enabling only a part of the manipulation means that is associated with a data size of the specified operand,

wherein the manipulation control means decodes the instruction, thereby obtaining size information about the data size of the operand that has been specified by the instruction and enabling only a part of the manipulation means that is specified by the size information,

wherein the manipulation means comprises register means for retaining operand data and size information about the size of the operand data, the operand data and the size information are retained in pairs, in the register means,

wherein if the manipulation control means has decoded a first instruction requesting that operand data of a particular size be written on the register means and has obtained size information about the data size of the operand specified by the first instruction, then the manipulation control means makes the register means retain not only the operand data but also the size information, and

wherein if the manipulation control means has decoded a second instruction requesting that the operand data retained in the register means be referred to, then the manipulation control means reads out size information about the size of the operand data, as well as the operand data itself, from the register means, and enables only a part of the manipulation means that is specified by the size information read out from the register means.

2. (Original) The processor of Claim 1, wherein the manipulation means comprises arithmetic and logical operation means for performing arithmetic and logical operations on operand data, the operation means having the bit width corresponding to the maximum size, and

wherein only a part of the operation means that is associated with the data size of the specified operand is enabled.

3. (Original) The processor of Claim 2, wherein the manipulation means further comprises means for conveying operation information among respective components of the arithmetic and logical operation means, and

wherein only a part of the conveying means that is associated with the data size of the specified operand is enabled.

4. (Original) The processor of Claim 3, wherein the operation information conveyed by the conveying means is information about carries.

5. (Canceled)

6. (Original) The processor of Claim 1, wherein the manipulation means comprises:

bus means for transferring operand data therethrough, the bus means having the bit width corresponding to the maximum size; and

driver means for driving the bus means, the driver means also having the bit width corresponding to the maximum size, and

wherein only a part of the driver means that is associated with the data size of the specified operand is enabled.

7. (Original) The processor of Claim 1, wherein the manipulation means comprises:

bus means for transferring operand data therethrough, the bus means having the bit width corresponding to the maximum size; and

latch means for latching the operand data on the bus means, the latch means also having the bit width corresponding to the maximum size, and

wherein only a part of the latch means that is associated with the data size of the specified operand is enabled.

8. (Original) The processor of Claim 1, wherein the manipulation means comprises extension means for extending the size of operand data, the extension means having the bit width corresponding to the maximum size, and

wherein only a part of the extension means that is associated with the data size of the specified operand is enabled.

9. (Original) The processor of Claim 1, which is a RISC type.

10-11. (Canceled)

12. (Previously presented) The processor of Claim 1, wherein the first instruction is either an instruction requesting that operand data be loaded from a memory into the register means or an instruction requesting that immediate operand data be transferred to the register means.

13. (Previously presented) The processor of Claim 1, wherein the second instruction includes an operation code field that does not contain any information specifying the data size of the operand.

14. (Original) The processor of Claim 12, wherein the second instruction is either an arithmetic and logical operation instruction requesting that the register means be referred to or an instruction requesting that the operand data be stored from the register means into the memory.

15. (Previously presented) The processor of Claim 1, wherein if the manipulation control means has decoded a third instruction requesting that operand data be changed into a particular size and has obtained new size information about the data size of the operand that has been specified by the third instruction, then the manipulation control means modifies the size information of the data that is retained in the register means and corresponds to the specified operand.

16. (Previously presented) The processor of Claim 1, wherein the first instruction includes an operation code field that contains sign information specifying whether operand data should be handled as signed data or unsigned data, and

wherein the register means retains the sign information representing whether the operand data is signed or unsigned, and

wherein if the manipulation control means has decoded the first instruction to obtain the sign information representing whether the operand, specified by the first instruction, is signed or unsigned, then the manipulation control means makes the register means retain not only the operand data but also the sign information, and

wherein if the manipulation control means has decoded the second instruction requesting

that the operand data retained in the register means be referred to, then the manipulation control means reads out the sign information representing whether the operand data is signed or unsigned, as well as the operand data itself, from the register means, and controls the manipulation means such that the second instruction is executed in accordance with the sign information read out.

17. (Original) The processor of Claim 16, wherein if the manipulation control means has decoded a fourth instruction requesting that signed operand data be changed into unsigned one, or vice versa, and has obtained new sign information representing whether the operand, specified by the fourth instruction, is signed or unsigned, then the manipulation control means modifies the sign information of the data that is retained in the register means and corresponds to the specified operand.

18. (Original) The processor of Claim 17, wherein the manipulation control means comprises:

an instruction decoder for decoding a given instruction; and

a controller for taking control of writing and reading the size information and the sign information onto/from the register means.

19. (Currently amended) A processor for handling data of multiple sizes, the processor comprising:

manipulation means for performing a manipulation on an operand, the manipulation and the operand both being specified by an instruction, the manipulation means having a bit width corresponding to a maximum one of the multiple sizes; and

manipulation control means for enabling only a part of the manipulation means that is

associated with a data size of the specified operand,

wherein the manipulation means comprises register means for retaining operand data and size information about the size of the operand data, the operand data and the size information are retained in pairs, in the register means.

20. (Previously presented) The processor of claim 19, wherein if the manipulation control means has decoded a first instruction requesting that operand data of a particular size be written on the register means and has obtained size information about the data size of the operand specified by the first instruction, then the manipulation control means makes the register means retain not only the operand data but also the size information.

21. (Previously presented) The processor of claim 20, wherein if the manipulation control means has decoded a second instruction requesting that the operand data retained in the register means be referred to, then the manipulation control means reads out size information about the size of the operand data, as well as the operand data itself, from the register means, and enables only a part of the manipulation means that is specified by the size information read out from the register means.